

WHAT IS CLAIMED IS:

1. A resist pattern formation method comprising:
coating a substrate with a resist material having a glass transition temperature that increases under irradiation by an energy beam;
forming a resist pattern by exposing and developing the resist material;
irradiating a surface of the resist pattern with the energy beam at a predetermined dosage to increase the glass transition temperature of upper parts of the resist pattern;
and
baking the resist pattern after irradiation by the energy beam, causing lower parts of the resist pattern to flow viscously so that the resist pattern assumes a tapered cross section.
2. The resist pattern formation method of claim 1, wherein the substrate is a semiconductor substrate.
3. The resist pattern formation method of claim 1, wherein the substrate includes an interlayer dielectric film.
4. The resist pattern formation method of claim 1, wherein the resist pattern is a contact hole pattern.
5. The resist pattern formation method of claim 1, wherein the resist pattern is a via hole pattern.
6. The resist pattern formation method of claim 1, wherein the resist pattern is a trench pattern.
7. The resist pattern formation method of claim 1, wherein the resist pattern is a damascene groove pattern.

8. The resist pattern formation method of claim 1, wherein the resist pattern is a capacitor pattern.

9. The resist pattern formation method of claim 1, wherein the energy beam is an electron beam.

10. A device fabrication method comprising:

coating a substrate with a resist material having a glass transition temperature that increases responsive to irradiation by an energy beam;

forming a resist pattern by exposing and developing the resist material;

irradiating a surface of the resist pattern with the energy beam at a predetermined dosage to increase the glass transition temperature of upper parts of the resist pattern;

baking the resist pattern after irradiation by the energy beam, causing lower parts of the resist pattern to flow viscously so that the resist pattern assumes a tapered cross section; and

forming a tapered feature in the substrate by etching the substrate by a process that simultaneously etches the tapered cross section of the resist pattern, the resist pattern functioning as an etching mask during the etching process.

11. The device fabrication method of claim 10, wherein the etched substrate is a semiconductor substrate.

12. The device fabrication method of claim 10, wherein the etched substrate is an interlayer dielectric film.

13. The device fabrication method of claim 10, wherein the tapered feature is a contact hole.

14. The device fabrication method of claim 10, wherein the tapered feature is a via hole.

15. The device fabrication method of claim 10, wherein the tapered feature is a trench.

16. The device fabrication method of claim 10, wherein the tapered feature is a damascene groove.

17. The device fabrication method of claim 10, wherein the tapered feature is a capacitor pattern.

18. The device fabrication method of claim 10, wherein the energy beam is an electron beam.